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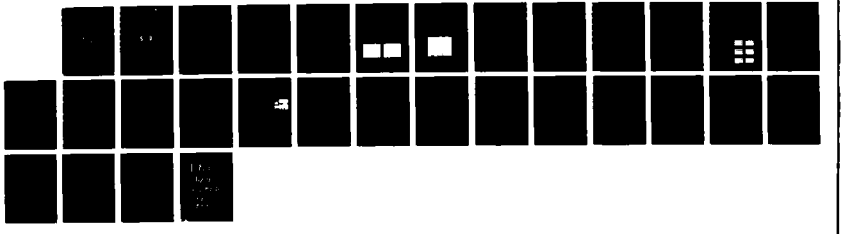

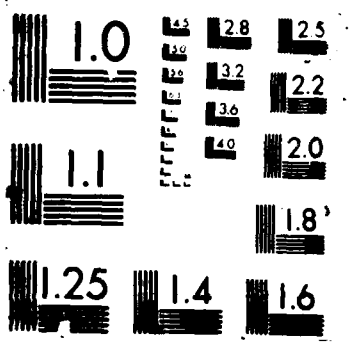
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PICOSECOND ELECTRONICS AND OPTOELECTRONICS

POSTDEADLINE PAPERS

JANUARY 14-16, 1987
INCLINE VILLAGE, NEVADA

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The purpose of this conference is to bring together workers in the areas of electronics and optoelectronics who share a common interest in the physics and technology of picosecond solid state devices, their multi-gigahertz applications and ultrafast measurement techniques. Subjects covered included: optoelectronic devices; semiconductor device physics; electronic devices; cryo-electronics; device fabrication technology; device characterization; and circuits and signal processing.

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Summaries of papers presented at the Picosecond Electronics and Optoelectronics Topical Meeting

January 14–16, 1987

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TOPICAL MEETING ON

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ERRATA

Reprinted copy of page 102 including Figures 2(a) and 2(b).

Reprinted copy of page 112 including Figure 2.

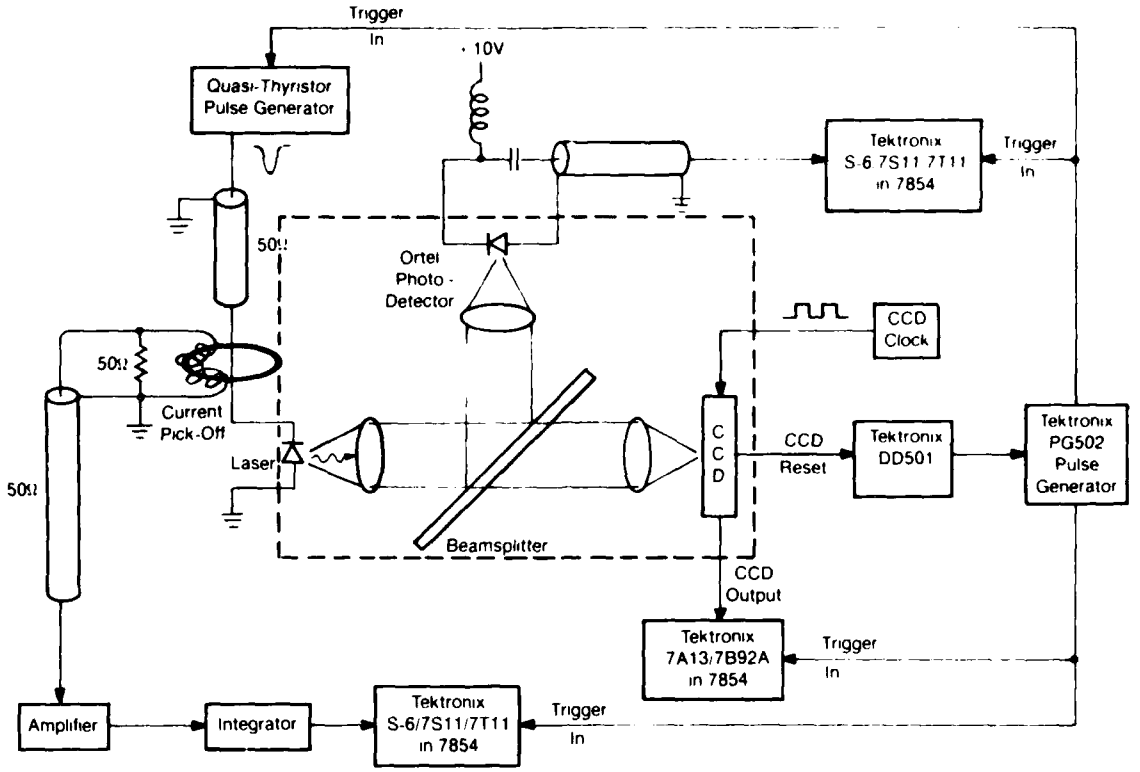


FIG. 1

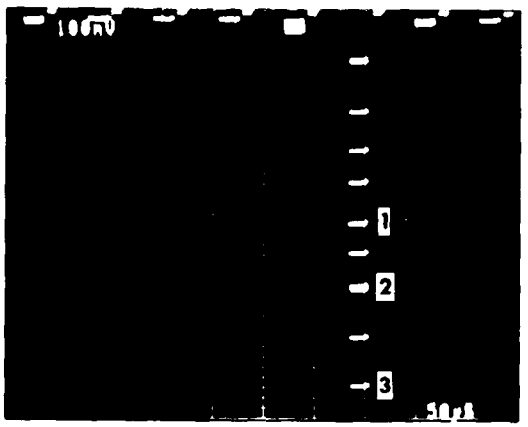


FIG. 2 (a)

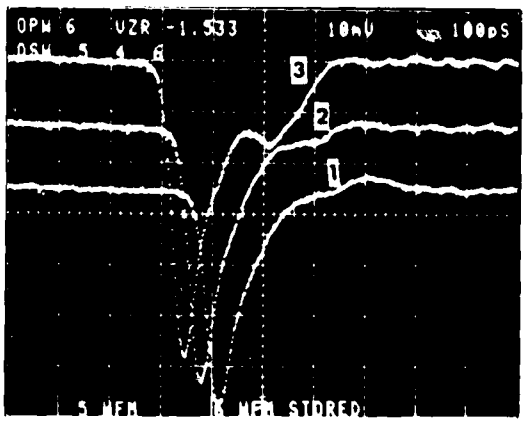


FIG. 2 (b)

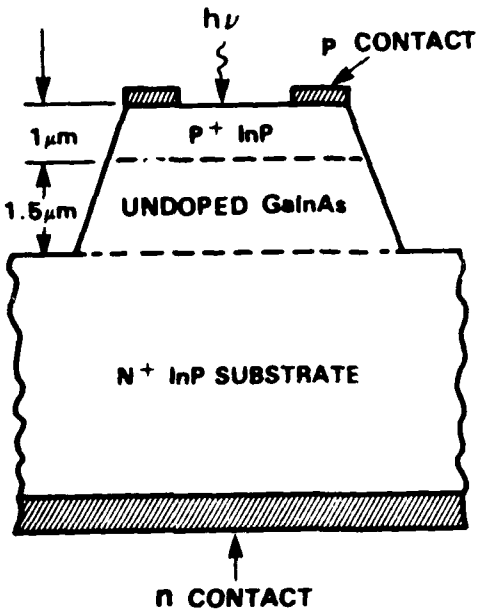
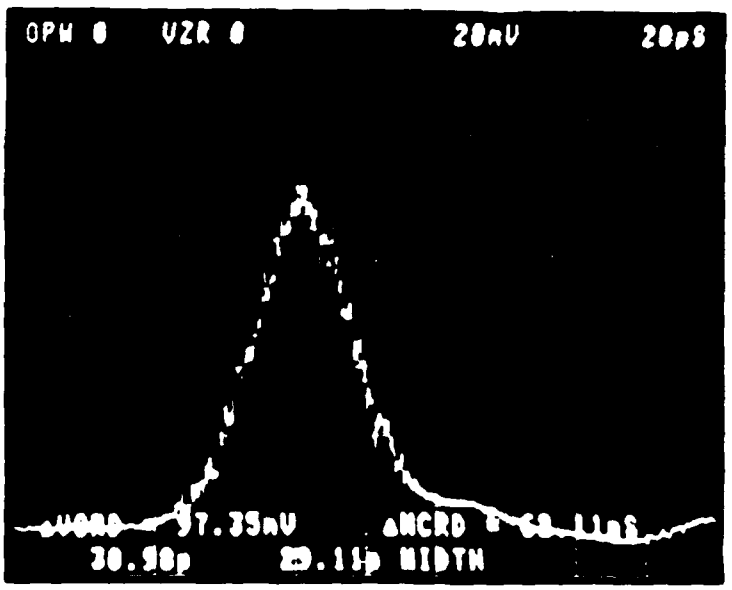


Figure 1:
Layer structure of the InP/GaInAs/InP front-side illuminated photodiode; the absorbing layer GaInAs is 1.5 μm thick, and the window layer P-InP is 1 μm thick. 1000 A SiO_x was used as antireflection. Photosensitive area is 25 μm in diameter in contact with a 25 μm diameter bondpad.



FWHM = 29 ps, 20 ps/DIV, 20 mV/DIV

Figure 2:
Transient time response of the photodiode to 1.3 μm diode laser pulse showing a full width at half maximum of 29 ps and a fall time of 31 ps. The impulse response of the sampling head is 23ps. Using a Gaussian approximation a combined photodiode and laser pulse width of 18 ps is calculated.

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Zhang, X-C. -- WE17

ELECTRO-OPTIC SAMPLING ANALYSIS OF TIMING PATTERNS AT CRITICAL INTERNAL NODES IN GIGABIT GaAs MULTIPLEXERS/DEMULTIPLEXERS

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Picosecond electro-optic sampling (EOS) has already been demonstrated by several researchers[1-4] to represent a unique capability for direct non-invasive probing of GaAs integrated circuits with high temporal resolution. In this presentation, we describe the use of this capability for a detailed analysis of on-chip waveforms at critical internal nodes in gigabit sequential logic circuits. Besides providing vital timing information between such internal nodes (and thereby providing the first clear measurements of timing parameters such as set-up and hold-times in flip-flops, and gate propagation delays in normally-loaded and normally-exercised gates), such EOS measurements report the first observation of effects such as clock feedthrough at internal nodes, as well as provide indispensable information on the accuracy of the modelling/simulations (typ. SPICE) that are usually done for the analysis of quirks in the internal behavior of such circuits.

The experimental arrangement is similar to that reported earlier[1,4], with ~ 3.5 picosecond pulses from a mode-locked and compressed YAG laser being used for the EOS measurements described here. All the measurements reported here were performed directly on wafers (obtained from GigaBit Logic, Inc.) with conventional probe cards used for biasing and feeding of the gigabit rate clock inputs. A clock frequency of 1.31 Gigahertz, synchronized to within a few Hertz of a precise integer multiple of the repetition rate of the mode-locked YAG laser, was used for all the data reported here.

Figure 1 shows the temporal resolution of our EOS system obtained from a GaAs FET which acts as a photodetector. Figures 2(a) and 2(b) show the circuit diagram of a falling edge triggered D-flip-flop (D-FF) and the waveforms observed at various internal nodes. From the timing relationships between such waveforms (measured on highly-expanded traces with ~ 2 psec resolution), set-up and hold times for the D-FF, as well as propagation delays for each of the six NOR gates comprising the D-FF, can be inferred very accurately. For instance, the propagation delay for gate A (fan-out = 3) and the set-up timing margin between the clock and data input AA were measured to be 97 ps and 190 ps respectively; from the smallest timing margin measured in this D-FF, we infer its maximum operational frequency as approximately 1.74 GHz.

Timing patterns corresponding to the 8 phases of a 4-stage Johnson counter (constructed with D-FF's similar to that described above) are shown in Figure 3, and strobe pulses, decoded from the Johnson counter outputs by a simple combinational logic circuit, are depicted in Figure 4. Such strobe pulses are used to control data combining and separation in 8-phase gigabit multiplexers and demultiplexers. Several of the "ripples" and "glitches" observed in Figures 1-3 are also observed in the SPICE simulations, and are

ascribable to simple effects, such as clock feedthrough; the slow ramping (with a time constant of a few nanoseconds) observed in the data is attributed to circuit parasitics. We will elaborate on these points in the presentation. Additional data will be presented, time permitting, and various practical aspects of EOS measurements in such circuits, such as voltage sensitivity, absolute voltage measurement, and the effect of crosstalk from adjacent signal bearing lines, will also be discussed.

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3. M.J.W. Rodwell, K.J. Weingarten, J.L. Freeman, and D.M. Bloom, Electron. Lett., 22, 499 (1986).
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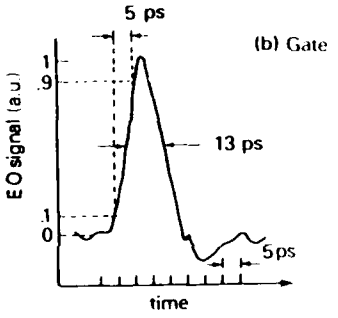
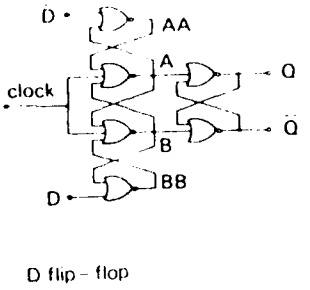


Fig. 1



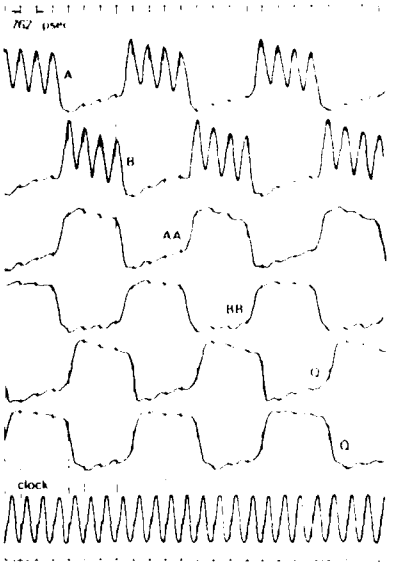


Fig. 2 (a) above
(b) right

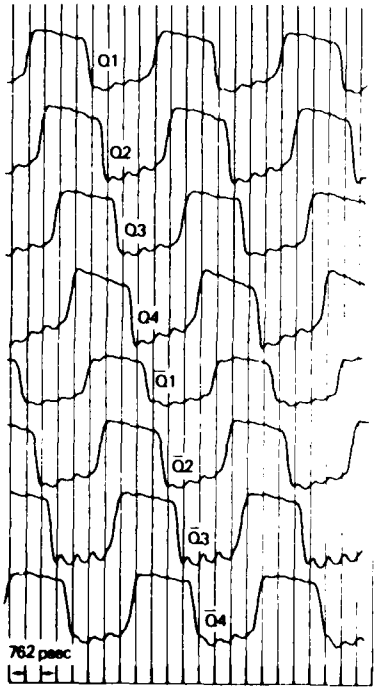


Fig. 3

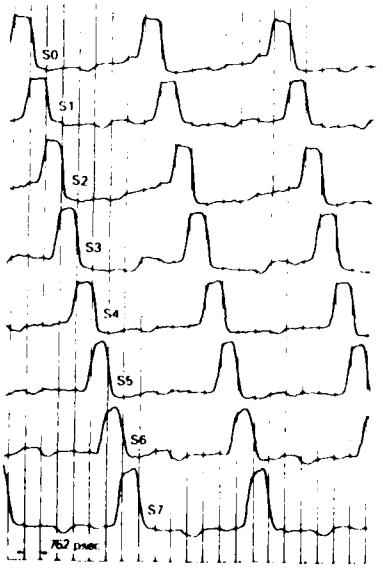


Fig. 4

16 Gbit/s Direct Modulation of an InGaAsP Laser

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Holmdel, New Jersey 07733

The fastest transmission systems demonstrated to date are at a bit rate of 8 Gbit/s [1,2]. Laser modulation experiments at 10 Gbit/s NRZ and 8 Gbit/s RZ were recently reported [3,4] as well as simulations using the highest frequency components of a 16 Gbit/s NRZ code [5,6]. Recent improvements in the cut-off frequency of FETs and increases in laser modulation bandwidth now allow the investigation of optical systems at higher speeds by electronically multiplexing pseudorandom 2 Gbit/s signals of length 2^{15}-1 into a 16 Gbit/s NRZ bit stream.

The experimental system is shown in Figure 1. The electronic input was an 8 Gbit/s NRZ bit stream created by multiplexing four pseudorandom 2 Gbit/s signals of length 2^{15}-1 [1]. The 8 Gbit/s signal was split into two identical signals using a broadband resistive divider, and one output was then delayed in a coaxial cable for 2.0 ns with respect to the other. Both signals were converted to RZ format by multiplying each against an 8 GHz sine wave in separate hybrid dual-gate GaAs FET circuits (small signal bandwidth of 18 GHz). The 8 Gbit/s RZ signals were resistively combined to produce the 16 Gbit/s NRZ signal shown at the top of Figure 2. This signal was then amplified in a hybrid GaAs FET driver circuit to provide up to 1.5 Vpp into 50 Ω, as shown in the middle of Figure 2.

The amplified multiplexer output drove a multilongitudinal-mode 1.3-μm-wavelength constricted mesa laser [7]. The laser threshold was 20 mA. The laser bandwidth increased linearly with the square root of optical power with a slope of 5.3 GHz/$mW^{1/2}$, and saturated with a maximum bandwidth of 15 GHz at an optical power of 10 mW and a current of 120 mA. The laser output was focused onto a high-speed PIN InGaAs/InP photodetector [8] with a bandwidth of 22 GHz, a quantum efficiency of 55% and a leakage current of 10 nA, all at a bias voltage of 5 V. The photodetector was connected directly to a Hewlett Packard 1430C sampling head (rise time < 20 ps) and the electrical waveforms were displayed on a Hewlett Packard 1811A sampling oscilloscope.

The detected optical output is shown at the bottom of Figure 2 for a bias current of 90 mA. The laser and detector cause some eye closure, but the center of the eye remains open. The bias dependence of the laser output was also examined. At the lowest biases single ones or even double ones do not turn on at all. At 40 mA bias, corresponding to 100% optical modulation, the laser rings by a factor of 2:1 during a long series of ones, and pattern effects are very significant. For 70 mA bias and above (optical extinction ratios of 2.9:1 and lower), the center of the eye is open. Previous experiments at 8 Gbit/s NRZ on similar lasers[1] showed that the lasers could be 100% modulated with open eyes. That is not true at 16 Gbit/s for similar driven levels (50 mA_{pp}). What drive level is needed for 100% modulation at these frequencies? Since most lasers have a small signal bandwidth/$power^{1/2}$ slope of approximately 4 GHz/$mW^{1/2}$, and since a small signal bandwidth of approximately 16 GHz is needed at the on-level, an on-level power of roughly 16 mW is required for 100% modulation. With a typical threshold of 20 mA and a typical (high power) quantum efficiency of 0.2 mW/mA/facet, this corresponds to an on-level current of 100 mA, and a required (ac-coupled) drive current of 80 mA for 100% optical modulation. Thus, 100% optical modulation at 16 Gbit/s appears likely, and even higher bit-rate modulation seems possible, provided the lasers are operated at higher currents, which means larger drive signals or smaller extinction ratios.

Acknowledgements

We gratefully acknowledge C. A. Burrus for supplying the high-speed PIN photodetector, and B. L. Kasper for his collaboration in the design of the laser drive circuit.

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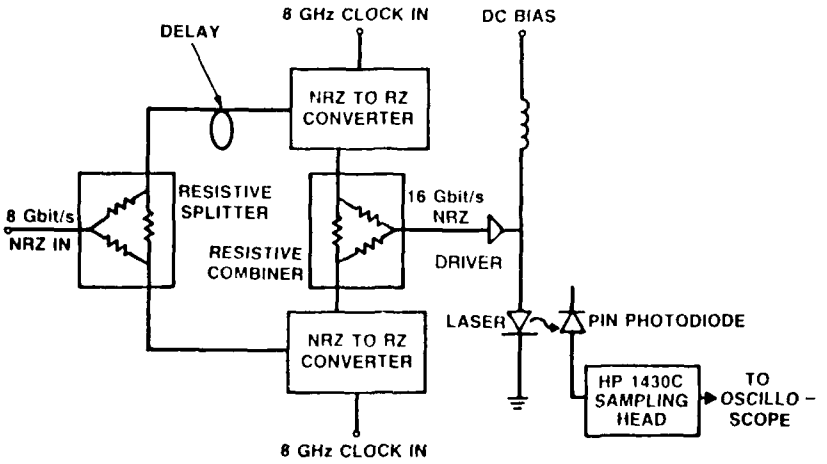

Figure 1: Schematic diagram of 16 Gbit/s modulation experiment.

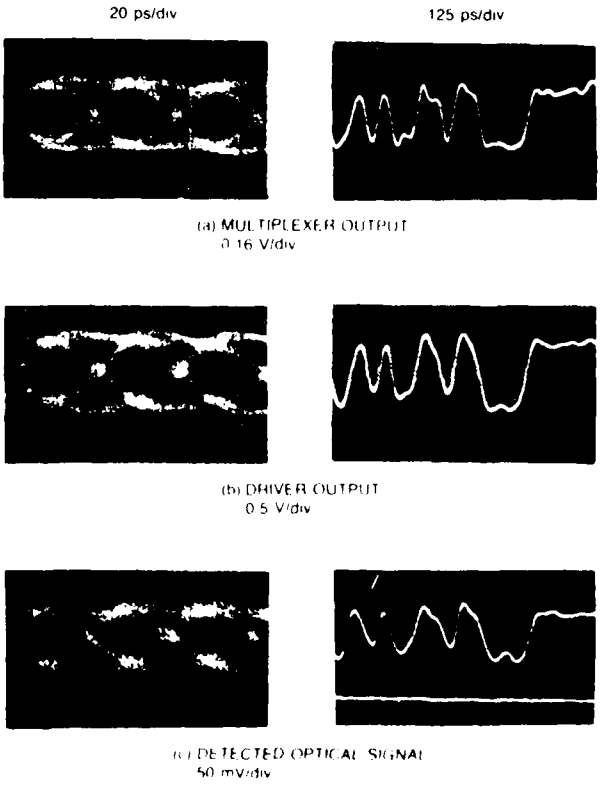

Figure 2: Sampling oscilloscope photos. Eye diagrams are shown at left. A portion of the bit pattern is shown on the right (00101001101100011111).

ADVANCES IN BIPOLAR IC TECHNOLOGY

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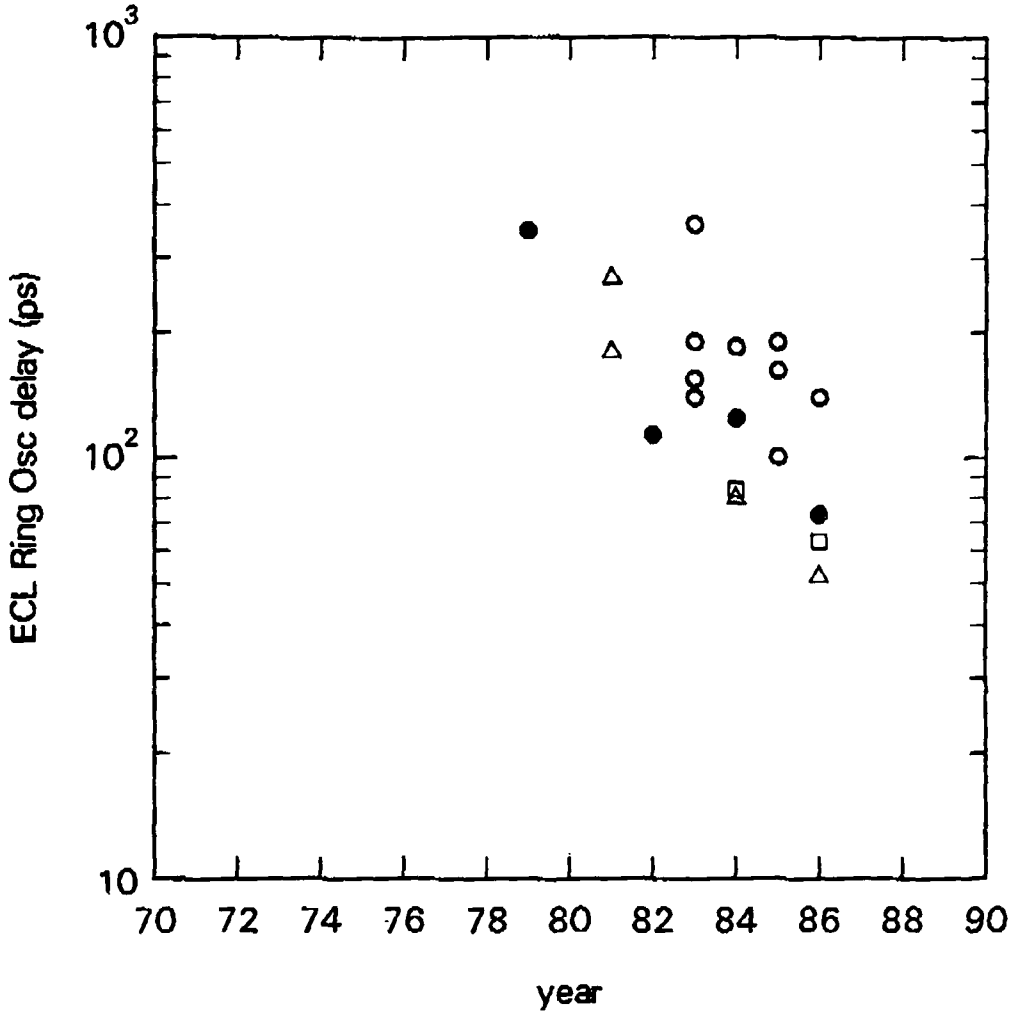
Si bipolar transistors and integrated circuits are widely used for high-performance gate arrays and high-speed cache memories, and have since become the backbone of the high speed computers. In recent years, steady improvements in the understanding of the design and scaling of the small dimension bipolar transistors together with the advances in the process technology have led to the realization of ever faster bipolar transistors and circuits.

Continued improvement in circuit performance is expected from scaling down to 0.25 μm dimension. The theoretical limit of scaling is reached when the base width is reduced to about 25 nm. At such a dimension, the mean free path of electron is comparable to the base width and the validity of the statistical drift-diffusion equation describing the device operation becomes questionable. Various second order effects in device physics which were of no concern in designing 2μm or larger devices now become important at one micron and sub-micron level. They are the heavy doping effects in the base, the reverse tunneling current, the contact to the shallow emitter and the base widening effects (Kirk-effects). Practical technology considerations such as the emitter resistance, the high current density at the emitter contact and electromigration may require deviations from following the scaling rules rigidly. Nevertheless, at sub-micron dimensions, even the partially-scaled bipolar devices (with wider base width) can yield circuit speeds approaching those presently achieved by the GaAs integrated circuits in an LSI environment.

Most of the advanced products are designed in 1.0 to 1.5 micron lithographic dimension. The technology development has been skewed toward improvement in circuit speed more than the integration level and is primarily dictated by the system requirement of the mainframe computer. Over the years, the most notable progresses are the introduction of. (1) self-aligned device structures, and (2) deep-groove isolation. The former ones improve the circuit speed and the latter improves the memory density and access time indirectly. The gate delay of the present ECL (Emitter-couple logic) circuits is in the range of a 0.25 - 0.50 nanosecond, and the typical gate array utilizes three levels of metal for wiring. A prototype gate array of 10,00 gates has been reported using four levels of metal.

The integration level of the bipolar memory increases at a rate much slower vs. MOSFET's. One reason is that the bipolar memory has been used predominantly as high-speed cache memory in mainframe computers where access time rather than density is of primary concern. The two most notable 64Kb prototype bipolar RAM chips are: (1) the MTL RAM with a chip power of 270mW and access time of 25 ns, designed with a conservative 2.2 μm lithography and fabricated using a junction isolation technology; (2) the 10ns 1.3W chip using deep-groove isolation and 1.2μm lithography. These two chips provide examples that the bipolar RAM's do not have to be high power to be fast.

It is expected that bipolar integrated circuits will continue to dominate the high-speed applications, especially the LSI logic gate arrays, and sub-100ps circuits will be available.



dots: IBM, square: SICOS(Hitachi), triangle:APSA (NEC).
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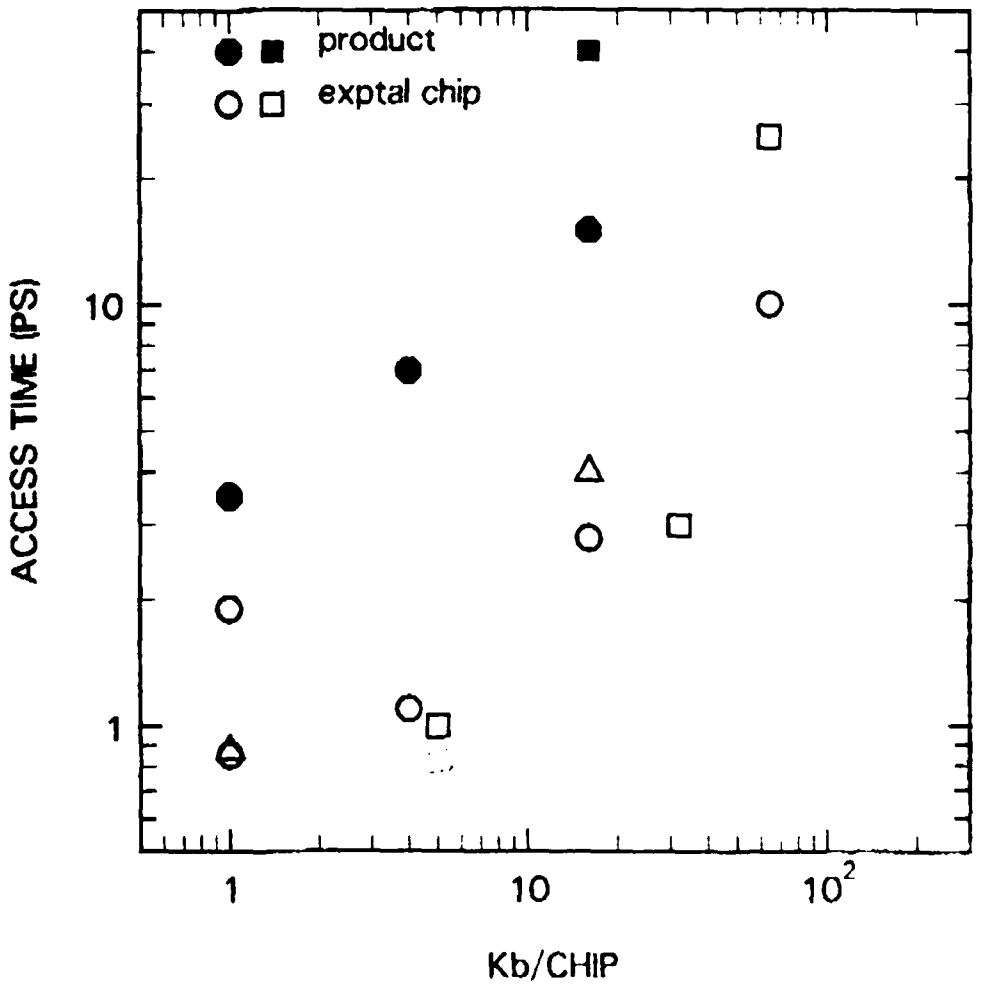
BIPOLAR MEMORY



Access time of bipolar Ram

triangles are data from HEMT (77 K)

D.D. Tang (5/86)

DEVELOPMENT OF 18 GHz GaAs STATIC FREQUENCY DIVIDERS AND THEIR EVALUATION BY ELECTROOPTIC SAMPLING

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INTRODUCTION

Digital integrated circuits (ICs) operating at clock rates above 10 GHz will have a significant impact on the performance of digital systems in the next decade. We have successfully employed advanced design and fabrication techniques to raise the operating frequency of room temperature GaAs MESFET divider circuits to 18 GHz, which exceeds speeds achieved by any other technology at any temperature.

Because of the limited bandwidth of conventional electronic instrumentation, measurement of digital performance above 10 GHz is generally a very formidable task. In this work, however, we have verified large signal digital operation and characterized signal timing on internal circuit nodes using electrooptic sampling techniques. Internal gate delay measurements from electrooptic sampling agree very well with gate delays estimated from the measurements of the maximum flip-flop toggle frequency.

FLIP-FLOP DESIGN AND FABRICATION

The divider circuits are implemented with a biphase master-slave flip-flop that has a maximum toggle rate of $1/2\tau_g$, where τ_g is the loaded AND/NOR gate delay. [1] Two logic families are used to implement the divider circuits. The first is the source-coupled buffered-FET logic (BFL) (Figure 1) [2]. BFL generally provides the fastest gate delay at high fanouts, but it also dissipates the most power per gate. The BFL gate employs only DFETs, so level-shifting is required to make input and output logic levels compatible. This extra circuitry increases both gate delay and power dissipation. However, the level-shifter stage also provides buffering to the following gate, and, therefore, has excellent fanout and interconnect drive capability.

An alternative to BFL in depletion mode technology is unbuffered source-coupled logic (CSL) (Figure 2) [3]. CSL uses diode level shifting to establish the operating points of the circuit, however, a reverse biased diode, which functions as a gate-to-source capacitor, is placed in parallel with the level shift diodes to speed up only the switching gates. During fast logic-state transitions, all the switching currents pass through the capacitor. Since the speed of the logic gate does not depend on the operating current in the level-shift diodes, this current can be minimized to achieve low power dissipation. The fanout capability of the CSL gate is not as high as the BFL because the output is not buffered, but at low fanout, CSL is potentially faster than BFL.

To maximize the speed of GaAs ICs, several issues are addressed. 1) The device and circuit design rules are reduced to provide submicrometer transistor gate lengths. 2) Shorter gatelengths require thin active channels (~700 Å) grown by MBE. 3) Source resistance is minimized by using n^+ contact layers grown on top of the channel, and 4) airbridge interconnects are used to reduce parasitic capacitances. Figure 3 is an SEM photomicrograph of a portion of a completed IC with 0.2 μm gates and airbridges. More complete fabrication details are given in Ref. [1].

TEST RESULTS

The dividers were tested at Stanford University on wafer using the electrooptic sampling test station [4]. The clock inputs were generated using a microwave frequency synthesizer set to an exact multiple of the laser pulse repetition rate, plus some small frequency offset. To improve the signal-to-noise ratio of the electrooptic detected signal, clock inputs were also pulse modulated at 10 MHz for synchronous detection. The clock signals were then amplified with a microwave amplifier to obtain a 2 V logic swing into 50 Ω. A 180° phase balun was used to generate the biphase signals, and bias tees were used to dc-offset the clock inputs to their optimum values.

Figure 4 shows the electrooptic sampled waveforms from a CSL divider circuit measured at a clock frequency of 12.1 GHz. The top waveform is the input signal measured internal to the divider circuit at the input of the master latch. The middle waveform is the Q bar output of the slave, which is fed back to the D input of the master. The bottom waveform is the Q output of the master latch. The measured waveforms verify the correct operation of the divider. The data at the D input arrive before the rising edge of the clock. After the rising edge of the clock, the master output changes state. The critical delay, that determines the toggle rate of the flip-flop is the time between the 50% point of the rising edge of the clock, to the 50% point of the rising or falling edge (whichever is longer) of the output waveform. As measured from the waveform, the delay is 20 ps to the rising edge, and 28 ps to the falling edge. In this case, the delay from the clock to the falling edge sets the toggle rate. The maximum toggle frequency of this divider was measured to be 17.8 GHz at 170 mW power dissipation, which corresponds to a calculated gate delay of 28 ps. The electrooptic sampled waveform therefore confirms correct operation at 17.8 GHz.

Electrooptic measurements are also used to determine the internal delays in the BFL divider circuits. These internal delays give us insight into improving divider circuit performance. Figure 5 is the measured electrooptic waveform of the clock, the high impedance node of the master output BFL gate (node A, Figure 1), and the level shifted source follower output of the same gate (node B, Figure 1). The delay, from the clock edge to the high impedance node is 13.6 ps. The delay from the high impedance node to the output is 12.1 ps. Comparing these delays to values reported previously for longer BFET gatelengths [4], we find that the delay between the clock input and the high impedance node scaled with gatelength, however, the delay through the level shifter and level shift diodes remained about the same. The latter is due to the fact that the RC delay of the resistance of the level shift diodes and the gate capacitance of the following stage. The speed of this divider circuit can be improved by reducing the level shift diode resistance. The maximum measured toggle frequency of the BFL divider was 14.05 GHz, with 658 mW power dissipation. This frequency corresponds to a calculated gate delay of 35.6 ps, which correlates well with the 37 ps measured gate delay. [1]

SUMMARY

Electrooptic sampling techniques have been used to evaluate the performance of ultrahigh-speed frequency dividers. Electrooptic testing is a powerful technique to both confirm operation of high-speed digital circuits on-wafer, and to provide insight into maximizing their performance.

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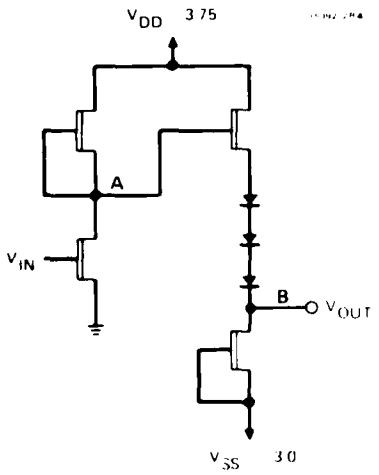

Figure 1. Buffered FET logic gate.

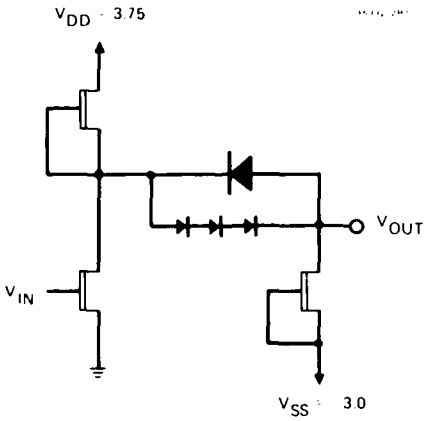

Figure 2. Capacitively enhanced logic gate.

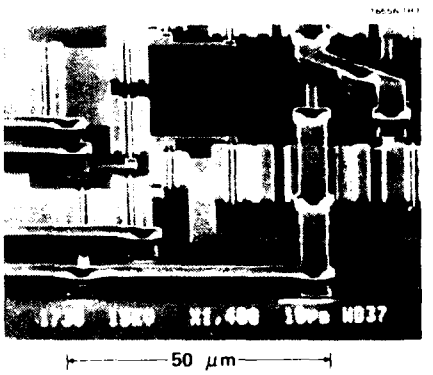

Figure 3. SEM photomicrograph of a completed divider circuit with 0.2 μm gates and airbridge.

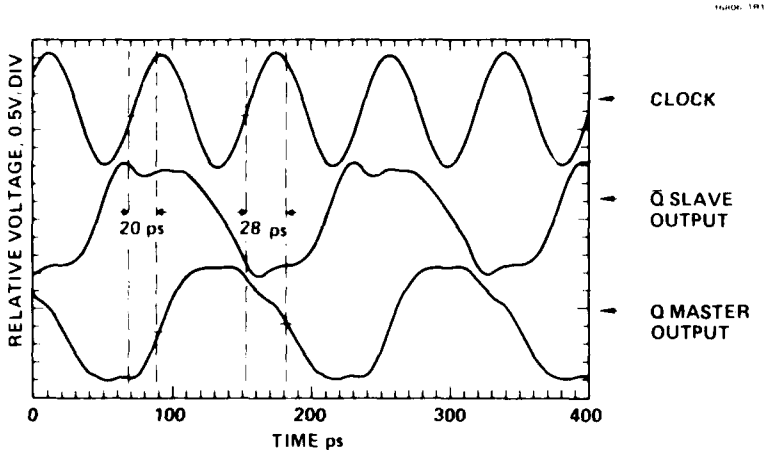

Figure 4. Electrooptic waveform from a CEL divider circuit measured at 12.1 GHz.

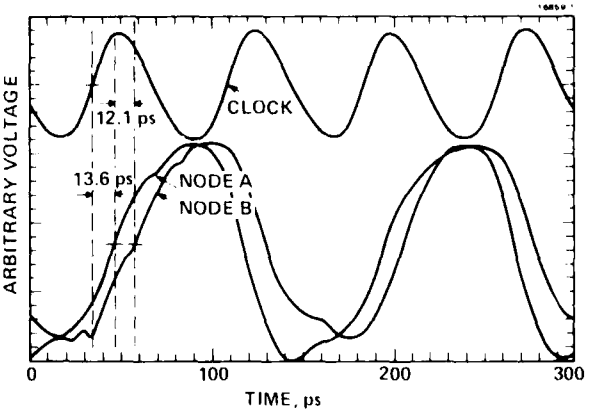

Figure 5. Electrooptic waveform measured at 13.46 GHz of the clock, high impedance point (node A), and source follower level shift output (node B) of a BFL divider.

Optical Reading of InGaAs Modulation Doped Field Effect Transistor

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We present the first observation of absorption quenching in a semiconductor quantum well by electrical control of the carrier density. We have observed this novel effect at room temperature in a single modulation-doped InGaAs quantum well which was used as the conducting channel of a field effect transistor (FET). The effect is extremely large and we have used it for direct optical determination of the state of the FET.

Modulation doping (MD) can be used to introduce carriers in QW [1], producing very high mobility materials well known for their application to high speed transport[2]. Because the carriers fill the two dimensional (2D) subbands up to the Fermi energy, the absorption edge is blue-shifted with respect to the luminescence emission[3], with a shift approximately proportional to the the number of carriers. Thus electrically-driven changes of the carrier density in a MD-QW will result in large changes in optical absorption. The conditions for the observation of this phenomenon correspond exactly to the situation encountered during the switching of a FET whose conducting channel is a MD-QW.

The structure we have investigated is a specially designed recessed gate InGaAs/InAlAs FET grown by molecular beam epitaxy (MBE) on InP:Fe. The structure is shown in Fig 1. It contains an $L_z = 100\text{Å}$ $In_{0.53}Ga_{0.47}As$ QW conducting channel for the 2D electron gas. The electrons are supplied by transfer through a 20Å $In_{0.52}Al_{0.48}As$ spacer layer from the 250Å $In_{0.52}Al_{0.48}As$ layer doped with $Si \sim 1.2\times10^{18}cm^{-3}$. The Schottky gate pattern consists of two bonding pads of 300Å Cr followed by 3000Å Au connected to a $1.6\times100\mu m$ active region which is centered in a $5.4\mu m$ gap between the source and the drain.

The InAlAs layers as well as the InP substrate are transparent around the InGaAs gap ($\lambda \approx 1.55\mu m$) making the device compatible with lightwave communication systems.

We measured the changes in absorption in the channel by illuminating the gate through the transparent substrate, and detecting the reflection from the metal gate, thus making two passes through the channel. The change in the intensity, ΔT , of the reflected beam was measured as function of the wavelength as the gate-source voltage was modulated. A set of typical spectra for gate-source voltage modulation $[(-0.6V) \rightarrow (-0.2V)$ and $(-0.6V) \rightarrow (+1.2V)]$ are shown in

Fig. 2. A large change is clearly seen at the position of the $n_z = 1$ exciton peaks. The profile of the difference spectrum corresponds to a decrease in absorption without shift of the exciton resonances. The maximum amplitude is $\Delta T \sim 2\%$. At the $n_z = 2$ resonance a somewhat weaker structure is also seen. The variation of absorption at this resonance has a completely different spectral profile which corresponds to a red shift of the $n_z = 2$ exciton peak due to band gap renormalization and the Quantum Confined Stark Effect.

Beside providing a wealth of information on the optical properties of MD-QW's, this effect has clear potential for monitoring and optically interconnecting electronic circuits based on III-V semiconductor technology. The effect is large enough to enable probing in a single QW and enables direct observations of the density of the conducting electron gas in the transistor. The contrast can be further increased in waveguides or by using more than one well.

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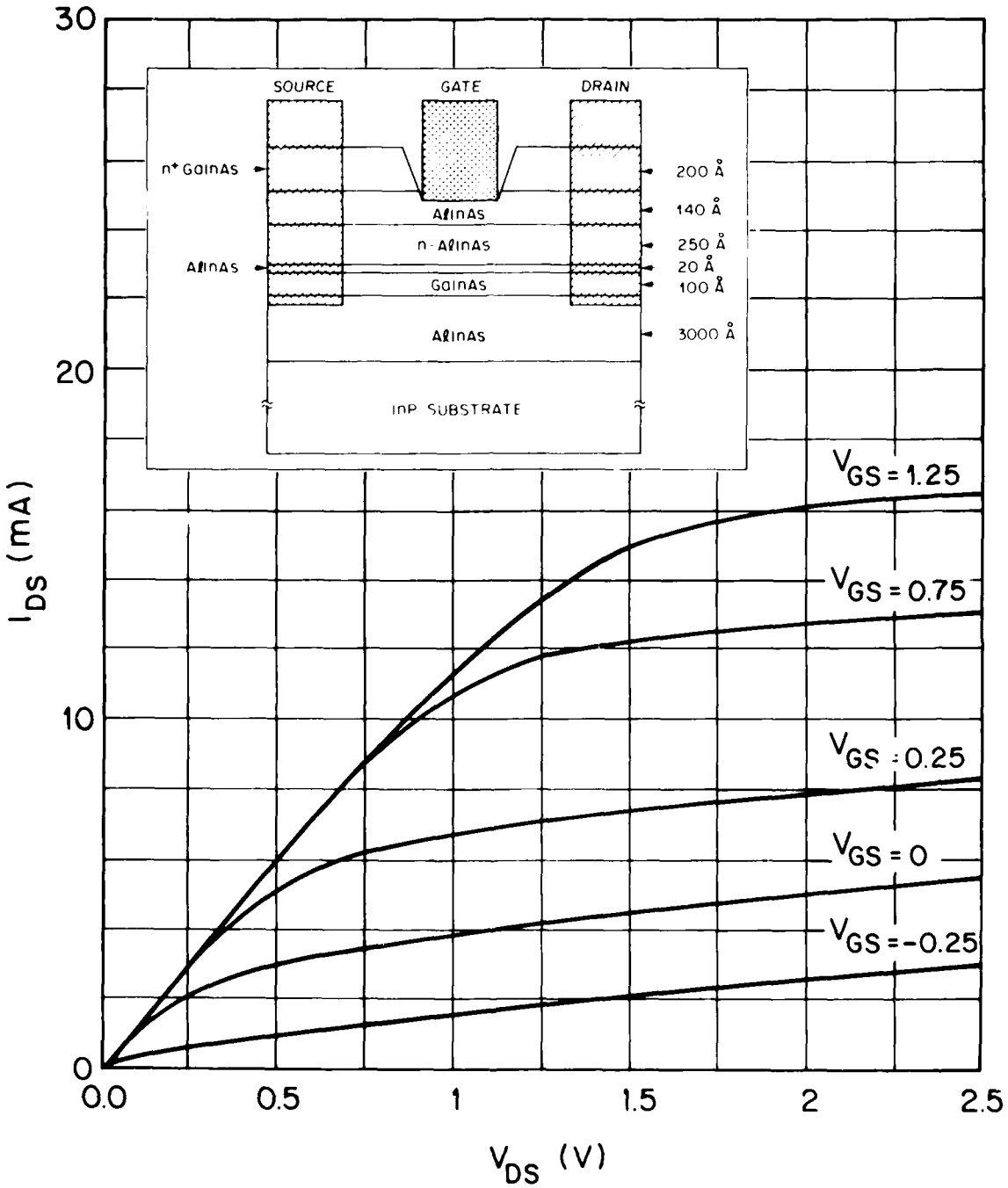
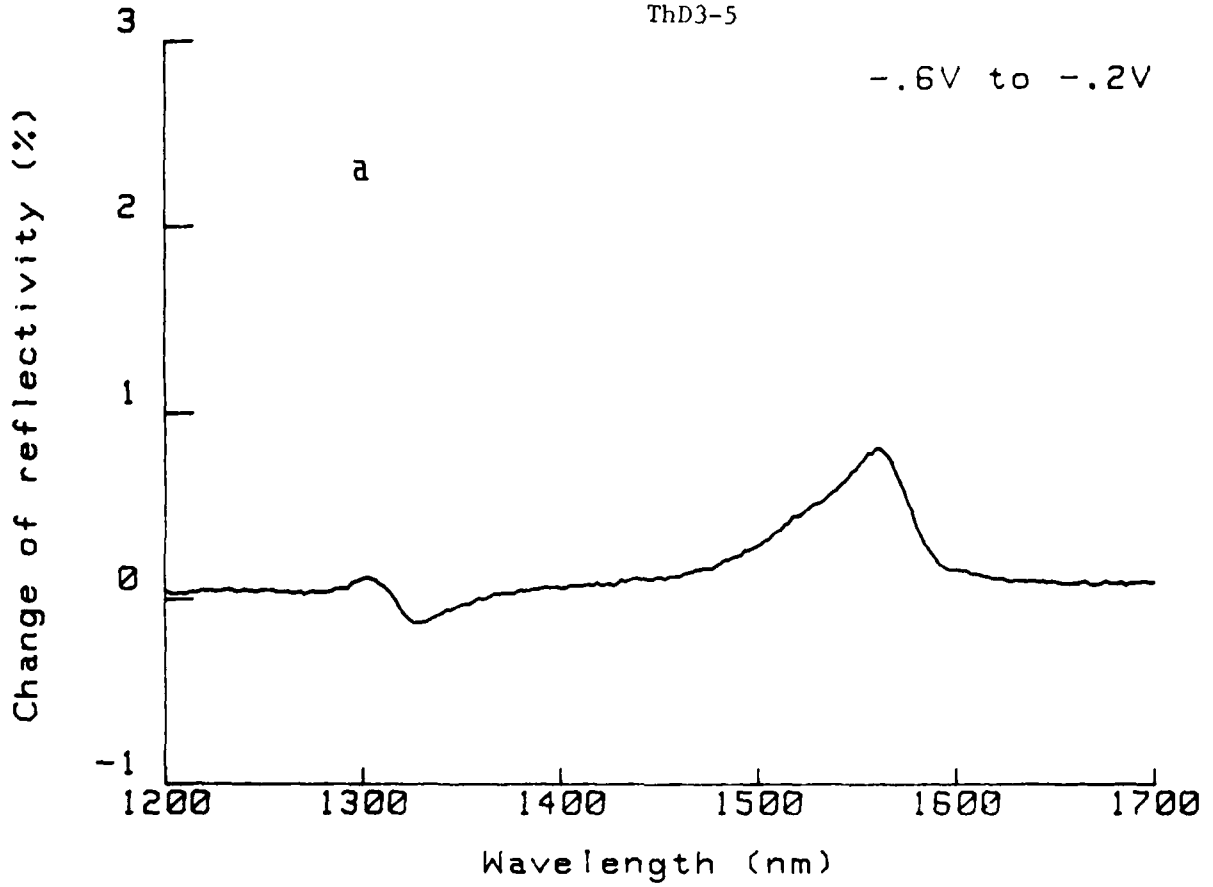
FIGURE CAPTIONS

Figure 1: Drain-source current/voltage characteristics of the InGaAs/InAlAs field effect transistor used in our experiments. The FET structure is shown in the insert.

Figure 2: Differential absorption spectra showing the absorption quenching of the $n_z = 1$ exciton resonances and the red shift of $n_z = 2$ resonance, for two gate voltage amplitudes: a) -0.6V to -0.2V . b) -0.6V to 1.2V.


SOURCE
GATE
DRAIN
n+ GaInAs
AlInAs
AlInAs
n- AlInAs
AlInAs
GaInAs
AlInAs
InP SUBSTRATE
200 Å
140 Å
250 Å
20 Å
100 Å
3000 Å
V_{GS} = 1.25
V_{GS} = 0.75
V_{GS} = 0.25
V_{GS} = 0
V_{GS} = -0.25
I_{DS} (mA)
V_{DS} (V)
0
10
20
30
0.0
0.5
1
1.5
2
2.5


-.6V to -.2V
a
Change of reflectivity (%)
3
2
1
0
-1
1200
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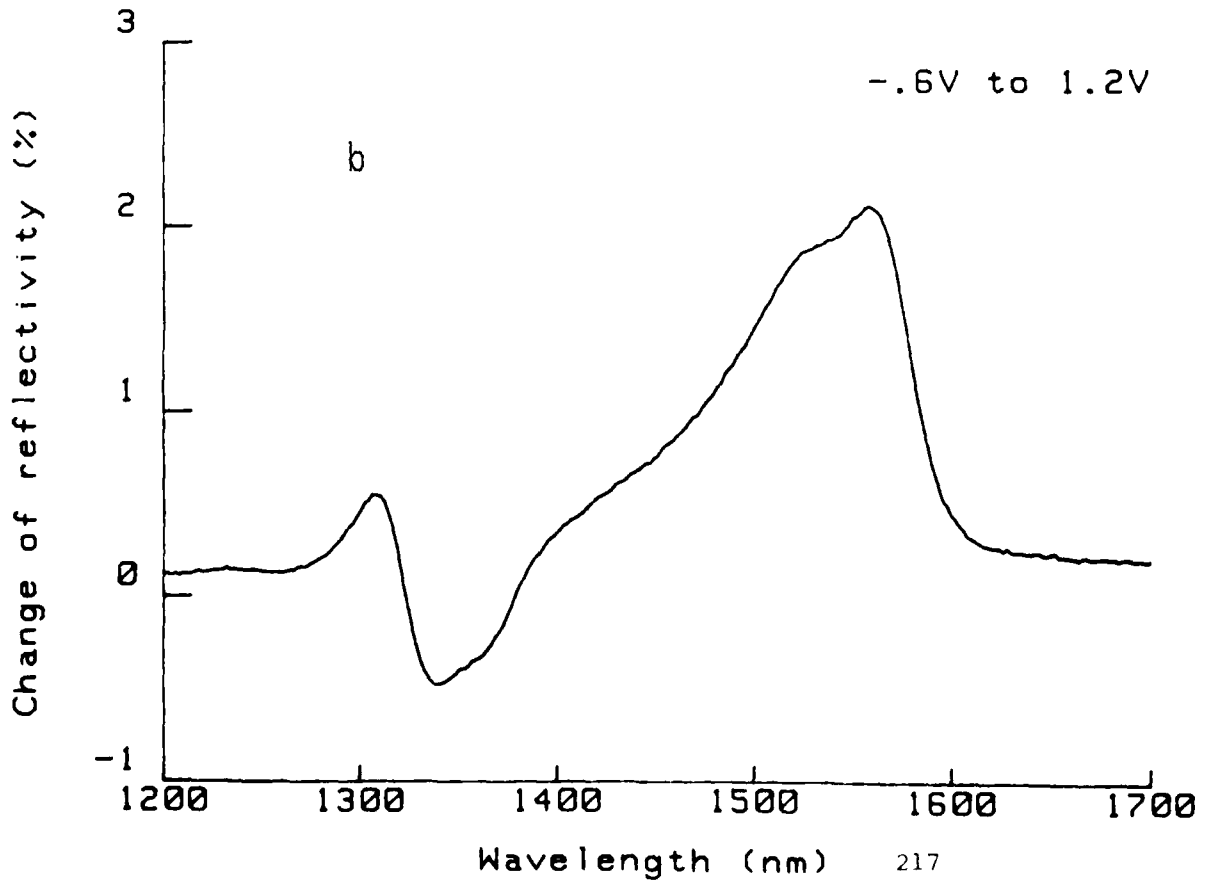
1500
1600
1700
Wavelength (nm)


-.6V to 1.2V
b
Change of reflectivity (%)
3
2
1
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1200
1300
1400
1500
1600
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Wavelength (nm)

Photoemissive Testing of High-Speed Electrical Waveforms

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Photoemissive sampling was recently introduced as a new, contactless method for probing high-speed electrical waveforms on circuits and devices on any semiconductor [1-3]. Previously the best temporal resolution achieved was limited to 40-psec. In this paper we describe photoemissive sampling measurements which demonstrate a temporal resolution below 7-psec.

Photoemissive sampling utilizes ultrashort optical pulses to stimulate the emission of photoelectrons from metal interconnection lines on the surface of the device under test; the potential at the emitting surface is derived by spectral analysis of the photoelectrons. Our experiments were performed with 2-eV, 80-fsec pulses from a colliding-pulse-modelocked ring dye laser, which generates photoelectrons via a three-photon photoelectric effect. A grid placed 400-μm above the sample provides an extraction field for the photoelectrons, which are subsequently detected using a microchannel plate detector (MCP). The energy analysis is accomplished by a retarding field analyzer mounted directly in front of the MCP.

The temporal resolution of photoemissive sampling is governed by the photoelectron transit time through the region of space in which the electric field depends significantly on the sample potential. This "effective transit time" T is given by:

$$T = \frac{\sqrt{2m}}{eE}\left[\sqrt{eES + U_o} - \sqrt{U_o}\right]$$

where E is the extraction field, m and e are the electron mass and charge, S is the spatial extent of the time-varying electric field, and U_o is the initial kinetic energy in the direction of the extraction field. The transit time may be reduced (and the temporal resolution improved) by using a high extraction field E and by minimizing the distance S. It should be realized that S is reduced when examining transmission line structures with a closely spaced signal line and ground plane (since the influence of the sample potential on the electric field above the sample is confined within a distance comparable to the signal line/ground plane separation) [4].

We performed photoemissive sampling measurements of electrical transients on a 5-μm gold coplanar stripline on GaAs. One optical pulse photoconductively generates a fast, ~200 mV

electrical step; a time-delayed probe beam generates photoelectrons from the center line of the stripline at a point 40-μm away from the origin of the electrical step. A time-resolved measurement of the potential at the probe position is shown in Fig. 1 for an extraction field of 25 KV/cm. The 10%-90% rise time is 7-psec; the steepest slope present on the rising edge would correspond to an even faster rise time of approximately 4-psec. For comparison, the calculated transit time is 3.6-psec, using S = 5-μm and U_o = 1 eV.

Our experiments demonstrate that photoemissive sampling is capable of probing 50 Ghz signals with a temporal resolution well below 10-psec.

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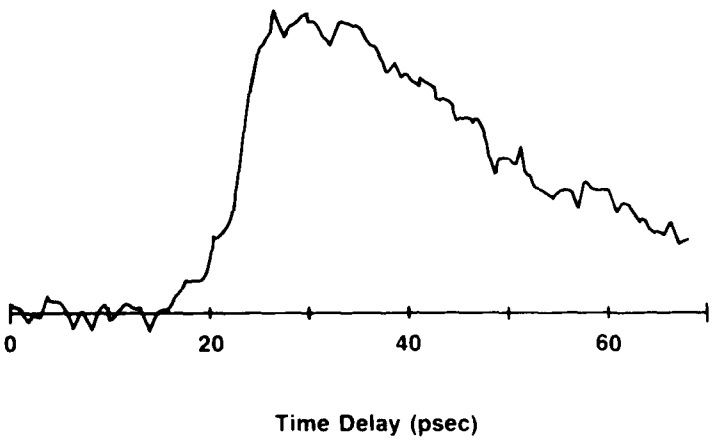

Fig. 1
Measured voltage waveform on a 5-μm coplanar stripline on GaAs.

Laser Pulsed E-Beam System for High Speed I.C. Testing.

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Electron probe techniques for the high speed testing of Integrated Circuits have considerably higher spatial resolution compared to optical techniques but have tended to suffer from poorer temporal resolution. In this presentation we describe a novel type of instrument that combines the advantages of conventional SEM voltage contrast techniques(1) (including a spatial resolution better than 0.1μm and beam steerability) with an order of magnitude improvement in temporal resolution.

Figure 1 shows a schematic of the system used. The thermionic gun or field emission gun of standard SEM systems is replaced by a thin film roughened gold photocathode deposited on a quartz substrate. The quadrupled output from a mode-locked Nd:YAG laser/fibre compressor arrangement is focussed onto the cathode (operating in transmission mode) which is mounted at the top of the SEM column. Because the photocathode is operated in transmission mode and the escape depth of the photoelectrons in gold is only a few 10's of angstroms then the film should be as thin as possible consistent with there being electrical continuity. Typically, 1ps pulses at 266nm, 100MHz and 2mW average power impinge on a 200A thick gold film which has an accelerating mesh in close proximity to reduce temporal spread produced by Coulomb interactions. The photoelectron yield is $0.5 10^{-3}$, which gives about 10,000 electrons per pulse.

The average brightness of the photocathode is quite sufficient to see real time 2-D images of samples under test, which is necessary so that a stationary spot beam can be easily positioned at the waveform measuring point for voltage measurements (or alternatively for 2-D time resolved voltage measurements). In addition the peak brightness is much larger than in beam blanked SEM systems which results in shorter sampling times. An especially designed in-lens energy spectrometer with an extraction and a retarding grid analyses the emitted secondary electrons (whose energy depends on

the voltage at the emission point) and allows close working distances for good spatial resolution. Using phase sensitive detection, voltage resolutions of better than $20mV/(Hz)^{1/2}$ have been achieved compared to $10mV/(Hz)^{1/2}$ when the thermionic source is used.

For time resolved measurements, part of the light beam incident on the photocathode is used as a trigger for the electrical signal whose waveform is to be measured, and the waveform is sampled by variably delaying the cathode incident beam with respect to the trigger. When looking at internal nodes on a clock-driven integrated circuit then the light signal is used to drive the clock in synchronism (less than 1ps jitter is achievable) with the electron pulse.

Figure 2 shows a sampled waveform derived from a step-recovery diode. A pulse generator, triggered by a photodiode signal from part of the light beam, provides an approximately sinusoidal signal at 100MHz to the step recovery diode. The resultant pulse measured with a sampling scope has a rise time of 60ps and a 5V peak amplitude. The electrical pulse is launched onto a 50 Ohm transmission line within the chamber where it is probed by the electron beam (primary beam energy of 2keV). The rise time of the resultant waveform, limited by the device, is under 50ps, which implies an instrument resolution better than 20ps. Though the line geometry is large (1mm) a small extraction field of 170V/mm is sufficient to achieve this time resolution; for smaller extraction fields the rise time measured increases due to the transient local field effect on the emitted secondary electrons. Monte Carlo simulations for safe extraction fields of 2kV/cm and for coplanar lines with micron geometries support a predicted instrument resolution of order 5ps.

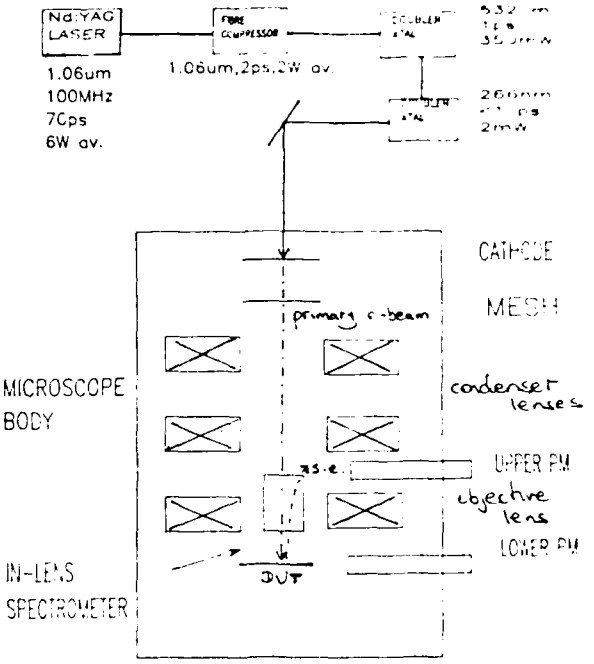

Figure 1: Schematic of Photoelectron Electron Microscope

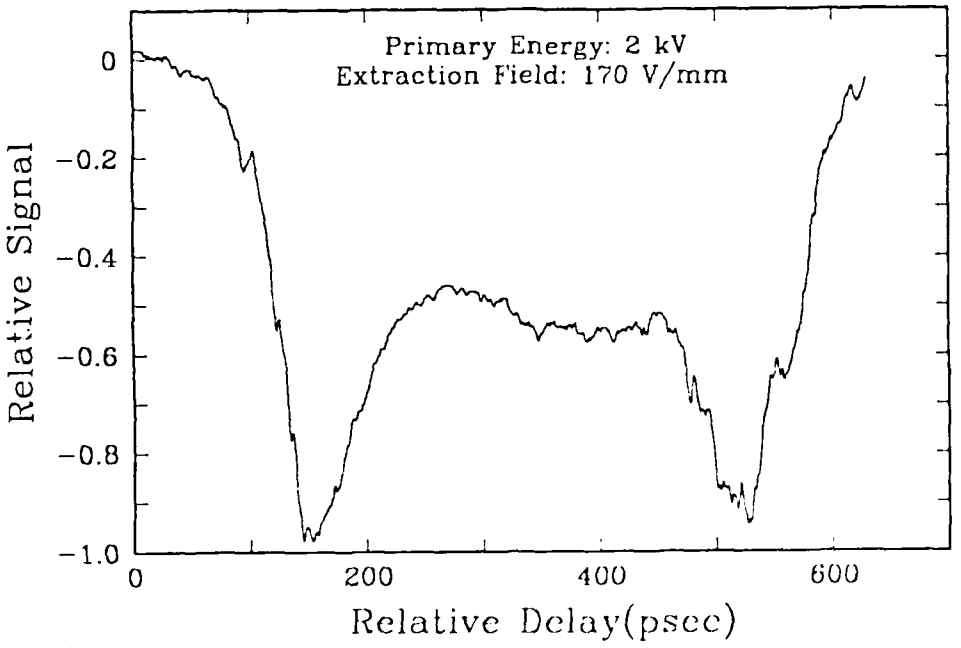

Figure 2: Measured waveform from step-recovery diode pulse launched on transmission line. The second peak comes from a reflection at a right angle bend in the transmission line.

References:

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A New 10 μm Infrared Detector Using Intersubband Absorption in Resonant Tunneling GaAlAs Superlattices

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The fabrication of 10 μm infrared detectors from III-V materials would allow advantageous use of their highly developed growth and processing technologies, as compared with II-VI compounds.[1-2] Furthermore, device parameters (e.g. bandgap, operating temperature, bandwidth and speed) can be tailored in ways that are difficult to do with either II-VI's or extrinsic Si detectors. We report here the first demonstration of a novel high speed infrared detector based on intersubband absorption and sequential resonant tunneling in doped GaAs/$Al_xGa_{1-x}As$ quantum well superlattices. We achieved a responsivity of 0.52 A/W at λ = 10.8 μm, an advantageous narrow bandwidth response $\Delta\lambda/\lambda \sim$ 10%, and estimate the speed to be $\approx$ 45 psec. From our experiments we have determined that the mean free path of the photogenerated hot electrons through the superlattice is 2500 Å.

The superlattice consisted of 90 Å $Al_{.24}Ga_{.76}As$ barriers and 65 Å GaAs wells (doped 1.4×10^{18} cm^{-3}). Detectors were fabricated by etching 50 μm mesas and back illuminating them through a 45° angle polished on the substrate. The responsivity vs bias voltage is shown in Fig. 1 for λ = 10.8 μm. The solid line is theory based on absorption of the infrared light by the intersubband resonance, followed by the rapid tunneling of the photoexcited electron out of the well in 10^{-14} sec, (shown in Fig. 2). The hot electron then travels a mean free path L (determined to be L = 2500 Å) thereby producing a photocurrent before being recaptured by one of the wells. As expected the detector response was found to be highly polarized and have a narrow spectral sensitivity.

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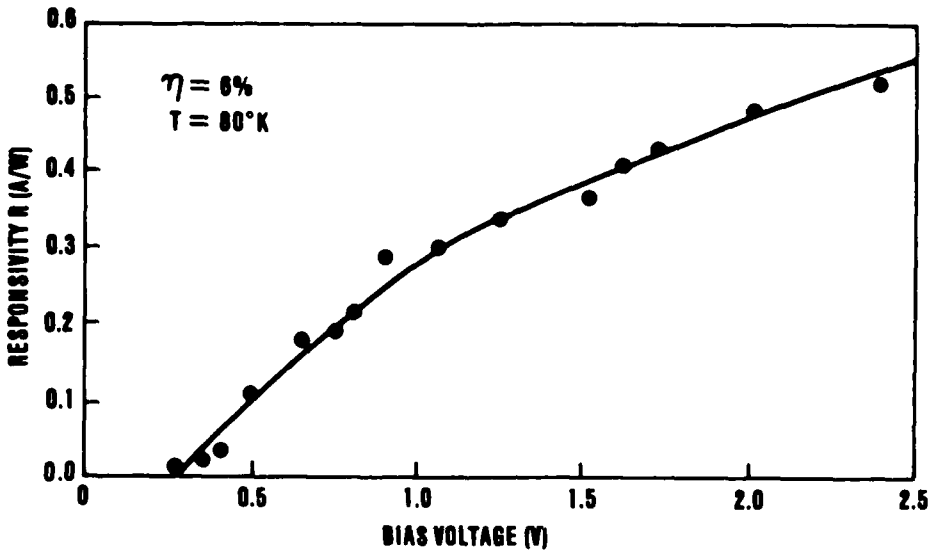

FIGURE 1

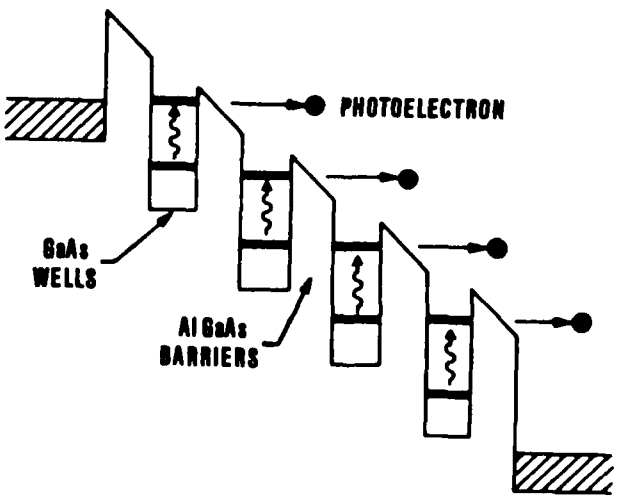

FIGURE 2

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